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㉕ INPUT SIGNAL DETERMINATION SYSTEM.

㉖ An input signal determination system for determining whether the state of an ac input signal is on or off. An ac input signal (1) is input to a processor (21) via a photocoupler (13). The processor (21) counts the time in which the ac input signal (1) remains higher than a predetermined threshold level and the time in which it remains lower than the predetermined threshold level. When the counted number for the higher level is greater than a precalculated number, the ac input signal is determined to be on, and when the counted number for the lower level is greater than the precalculated number, the ac input signal (1) is determined to be off. This makes it possible to correctly determine the on/off state of ac input signals within short periods of time.

EP 0 332 705 A1

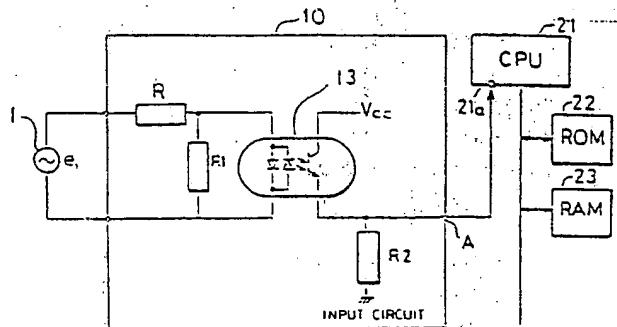


FIG. 1

## INPUT SIGNAL DISCRIMINATION METHOD

## Technical Field

The present invention relates to an input signal discrimination method for discriminating an AC input signal by a PLC (programmable logic controller) or the like, and more particularly to an input signal discrimination method for discriminating the state of an AC input signal by counting pulses.

## Background Art

Figure 4 shows an input circuit conventionally used to discriminate an AC input signal by a PLC or the like. In the figure, 1 represents an AC input signal, 10 represents an input circuit, and 20 represents a PLC for processing the input signal.

The input circuit 10 includes a rectifier circuit 11 for carrying out a full-wave rectification of the input signal, a resistor R and a capacitor C for smoothing the signal, and a photocoupler 12 to which the smoothed signal is supplied, to thereby separate a DC output from the AC input signal 1. A resistor R1, in cooperation with the resistor R, divides the voltage of the AC input signal 1 to lower the output level. The PLC discriminates the state, and carries out a sequence processing, of the AC input signal 1, based on the signal from the photocoupler 12.

With this circuit configuration, however, the output of the input circuit 10 must be a ripple-free signal, and therefore, the time constant  $R1 \cdot C$  of the circuit must be large. As a result, the response time of the input circuit 10 is prolonged and it is difficult to obtain a value shorter than three cycles of the alternating current of the AC input signal.

## Disclosure of the Invention

The object of the present invention is to provide an input signal discrimination method which solves the above-mentioned problem and in which the state of an AC input signal is discriminated by counting pulses.

To solve the above problem, the present invention provides an input signal discrimination method of discriminating an AC input signal, comprising: carrying out a pulse count in a time for which the AC input signal remains above a predetermined threshold level and a time for which the AC input signal remains below the predetermined threshold

level;

deciding that the AC input signal is on when the number of pulses counted while the AC input signal remains above the predetermined threshold level is larger than a previously calculated number of pulses; and

deciding that the AC input signal is off when the number of pulses counted while the AC input signal remains below the predetermined threshold level is larger than a previously calculated number of pulses.

When the AC input signal is on, the signal level remains higher than the threshold level for a predetermined time, and therefore, this high-level time is discriminated by the number of pulses counted to discriminate the signal on state.

Alternatively, when the AC input signal is off, the signal level remains lower than the threshold level for a predetermined time, and therefore, this low-level time is discriminated by the number of pulses counted to discriminate the signal off state.

## Brief Description of the Drawings

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FIG. 1 is a block diagram illustrating an embodiment of the present invention;

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FIG. 2 is a timing chart for illustrating the embodiment of the invention;

FIG. 3 is a flowchart illustrating the embodiment of the invention; and

FIG. 4 is a diagram showing an example of conventional input circuit.

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## Best Mode of Carrying Out the Invention

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An embodiment of the present invention will be described with reference to the drawings.

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FIG. 1 is a block diagram illustrating an embodiment of the present invention. In the figure, 1 denotes an AC input signal, the on or off state of which is determined by the effective value thereof, and 10 represents an input circuit which receives the AC input signal 1 and outputs a DC signal. The input circuit 10 includes resistors R and R1 which carry out a voltage division of the input signal and apply the divided voltage to a photocoupler 13. The photocoupler 13 includes light-emitting diodes connected in an inverse-parallel fashion as shown in the figure, for turning on a transistor when a current having a level higher than the threshold level flows in either direction. Vcc designates a voltage ap-

plied to a logic circuit and is usually + 5 V, and R2 denotes a voltage detection resistor. Accordingly, the input circuit outputs, from an output terminal A thereof, a signal obtained by carrying out a full-wave rectification of the AC input signal 1. Numeral 21 denotes a processor of a PLC (programmable logic controller) for global control of the PLC, 22 denotes a ROM for storing a monitor program for the PLC, a sequence program, and the like, and 23 denotes a RAM for storing various data and a signal output from the input circuit 10 through the processor 21.

The output of the input circuit 10, which is connected to an input port of the processor 21, is read by the processor 21 in a cycle shorter than one cycle of the AC input signal 1. When the AC input signal 1 is on, the output level of the input circuit 10 remains higher than the threshold level for longer than a predetermined time, and accordingly, the signal on time is prolonged. When the AC input signal is off, the time for which the output level remains below the threshold level is prolonged, and therefore, this time is counted by the processor to discriminate the state of the AC input signal.

FIG. 2 is a timing chart illustrating the embodiment of the invention. In the figure, C1 represents the AC input signal 1 in FIG. 1, and C2 represents the voltage across the resistor R1. The ratio of magnitude between the two is actually about 20:1 although the ratio illustrated is about 2:1. Straight lines L1 and L2 indicate the threshold levels of the photocoupler 13, OUTPUT OF INPUT CIRCUIT indicates the output waveform at terminal A of the input circuit 10 in FIG. 1, and READ CYCLE represents the timing at which the processor 21 reads the output signal of the input circuit 10.

When the AC input signal 1 is on, the voltage C2 across the resistor R1 exceeds and remains higher than the threshold level for longer than a predetermined time. Accordingly, if the input signal is read by the processor 21 in the above-mentioned read cycle, the on state continues for longer than a predetermined time, and as a result, the processor 21 decides that the input signal is on.

When the AC input signal 1 is off, the voltage across the resistor R1 is below the threshold level, or if higher than the threshold level, the time for which the voltage remains above the threshold level is shorter than a predetermined time. Therefore, the off time of the output signal of the input circuit is prolonged, and when the signal is read by the processor 21 in the read cycle mentioned above, the off state continues for longer than a predetermined time, and as a result, the processor decides that the input signal is off.

Referring to FIG. 2, assuming that the curve C2 represents the boundary between the signal on and

off states, then

$$ts = (1/N) \cdot tx = (1/n) \cdot Th$$

stands, wherein

ts: the interval of the read cycle of the processor;

5 N: the time for which the on state of the AC input signal continues;

Th: the half cycle of the AC input signal;

n: the number of read cycles during one half cycle of the AC input signal.

10 Namely, when the input signal remains on for longer than a time N, the processor decides that the AC input signal 1 is on. Alternatively, when the input signal remains off for longer than a time (n-N+1), then it is determined that the AC input signal is off.

15 Accordingly, the processor 21 can discriminate the state of the AC input signal within the time (Th+tx), and of the resistor R, thus forming a similar circuitry.

20 Moreover, the signal from the input circuit may be connected to the input port of the processor through a bus. Such a construction is particularly practical when the number of input signals is large, because the number of input ports is relatively small.

25 As described above, the construction of the present invention is such that the state of the AC input signal is discriminated by counting pulses, and accordingly, the response time is shortened and components such as a capacitor or the like can be omitted.

## Claims

35 1. An input signal discrimination method of discriminating an AC input signal, comprising: carrying out a pulse count in a time for which the AC input signal remains above a predetermined threshold level and a time for which the AC input signal remains below said predetermined threshold level;

40 deciding that the AC input signal is on when the number of pulses counted while the AC input signal remains above said predetermined threshold level is larger than a previously calculated number of pulses; and

45 deciding that the AC input signal is off when the number of pulses counted while the AC input signal remains below said predetermined threshold level is larger than a previously calculated number of pulses.

50 2. An input signal discrimination method according to claim 1, wherein said AC input signal is separated from a discrimination circuit by a photocoupler.

3. An input signal discrimination method according to claim 2, wherein said photocoupler includes light-emitting diodes connected in parallel and having opposite polarities.

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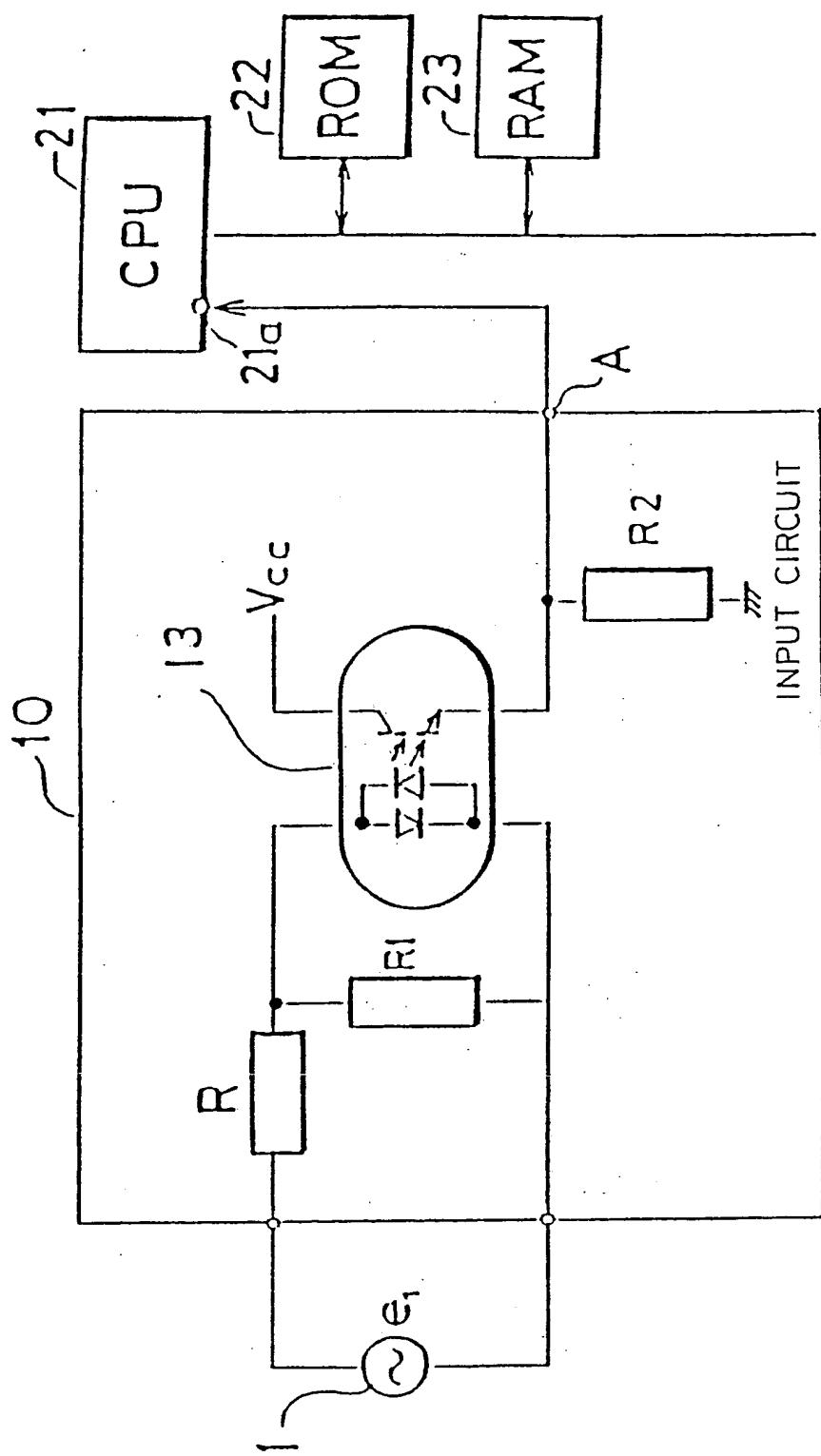


FIG. 1

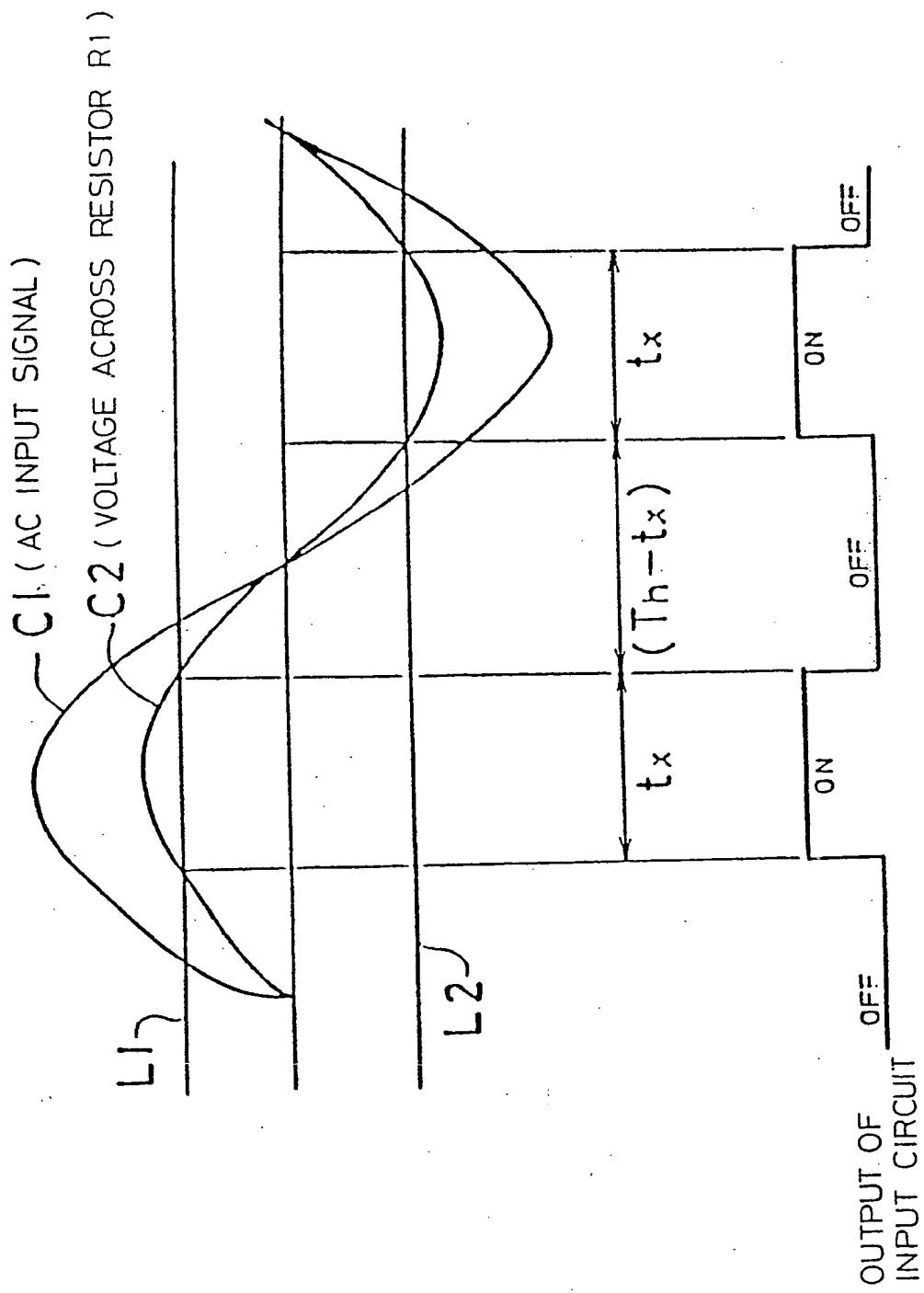
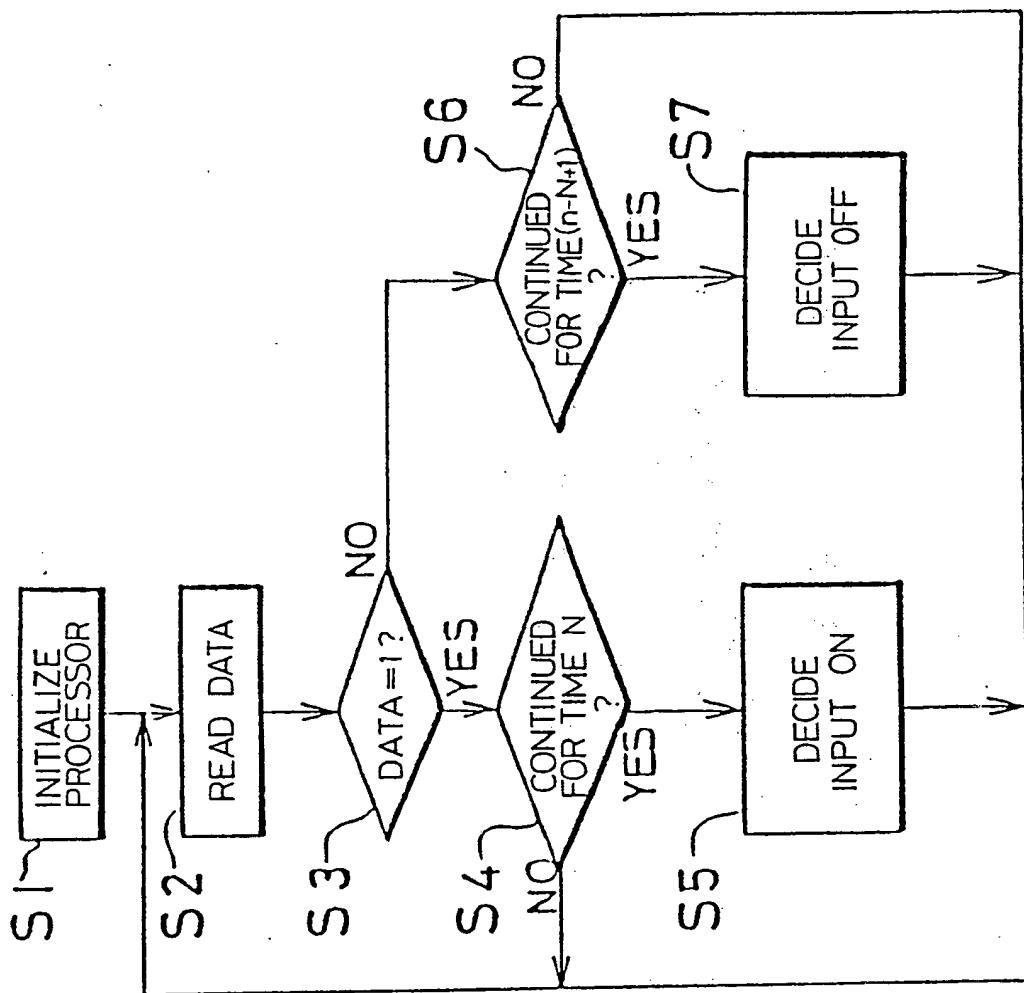


FIG. 2

FIG. 3



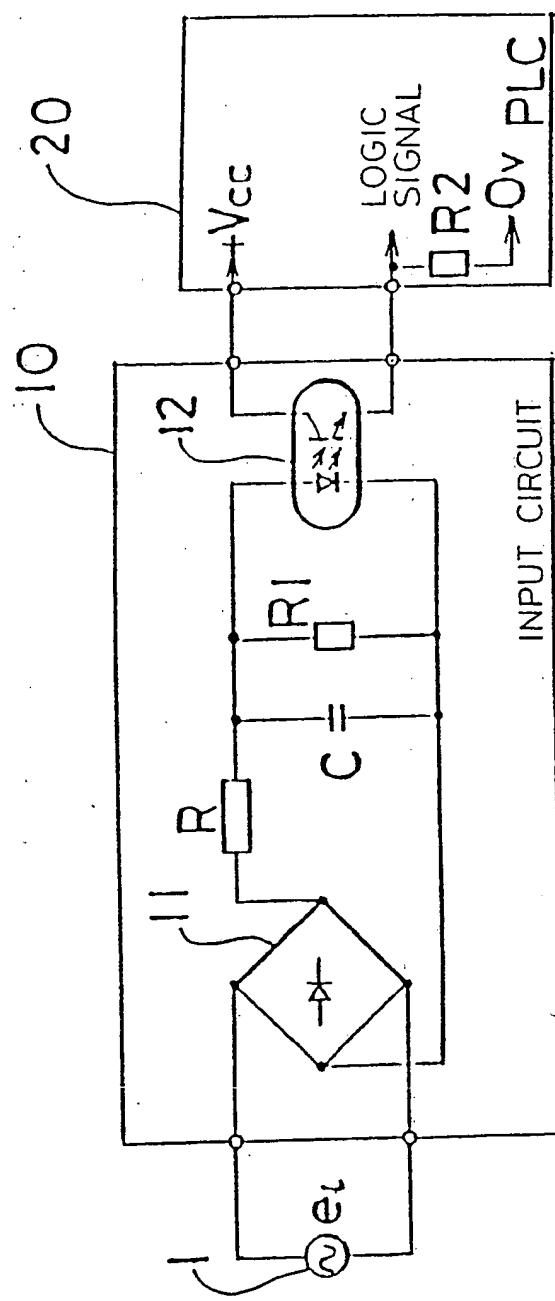


FIG. 4

## INTERNATIONAL SEARCH REPORT

International Application No

PCT/JP88/00191

## I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all)

According to International Patent Classification (IPC) or to both National Classification and IPC

Int. Cl<sup>4</sup> G01R19/165

## II. FIELDS SEARCHED

Minimum Documentation Searched<sup>7</sup>

| Classification System <sup>1</sup> | Classification Symbols |
|------------------------------------|------------------------|
| IPC                                | G01R19/00, 19/165      |

Documentation Searched other than Minimum Documentation  
to the Extent that such Documents are Included in the Fields Searched<sup>8</sup>Jitsuyo Shinan Koho 1926 - 1988  
Kokai Jitsuyo Shinan Koho 1971 - 1988

## III. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category <sup>9</sup> | Citation of Document, <sup>10</sup> with indication, where appropriate, of the relevant passages <sup>11</sup> | Relevant to Claim No. <sup>12</sup> |
|-----------------------|--|-------------------------------------|
| X                     | JP, A, 50-62735 (Omron Tateisi Electronics Co.)<br>28 May 1975 (28. 05. 75) (Family: none)                     | 1-3                                 |
| Y                     | JP, A, 50-122285 (Mitsubishi Electric Corporation)<br>25 September 1975 (25. 09. 75)<br>(Family: none)         | 1                                   |
| Y                     | JP, A, 54-83866 (Mitsubishi Electric Corporation)<br>4 July 1979 (04. 07. 79)<br>(Family: none)                | 1                                   |
| Y                     | JP, A, 53-3636 (Takeda Riken Kogyo Kabushiki Kaisha)<br>13 January 1978 (13. 01. 78)<br>(Family: none)         | 2, 3                                |
| A                     | JP, A, 50-127144 (Mitsubishi Electric Corporation)<br>6 October 1975 (06. 10. 75) (Family: none)               | 1                                   |

<sup>10</sup> Special categories of cited documents:<sup>11</sup> "A" document defining the general state of the art which is not considered to be of particular relevance<sup>12</sup> "E" earlier document but published on or after the international filing date<sup>13</sup> "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)<sup>14</sup> "O" document referring to an oral disclosure, use, exhibition or other means<sup>15</sup> "P" document published prior to the international filing date but later than the priority date claimed<sup>16</sup> "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention<sup>17</sup> "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step<sup>18</sup> "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art<sup>19</sup> "S" document member of the same patent family

## IV. CERTIFICATION

Date of the Actual Completion of the International Search

October 18, 1988 (18. 10. 88)

Date of Mailing of this International Search Report

November 7, 1988 (07. 11. 88)

International Searching Authority

Japanese Patent Office

Signature of Authorized Officer

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